termination structure using junctions. However, if the production is performed using each of the steps of a multi-epitaxial treatment, by stacking relatively thin junctions for individual epitaxial layers, the production is possible by only performing an ion implantation treatment using a normal-level implantation energy (e.g., about 700 KeV at most).

When source lead-out wires and gate lead-out wires are formed not over a portion having significant roughness due to trenches, but over a relatively planar substrate surface as in the foregoing embodiment, backing wiring using a metal can be used relatively easily so that it is easy to reduce the gate resistance or the like.

5. Summary

While the invention achieved by the present inventors has been specifically described heretofore based on the embodiment thereof, the present invention is not limited thereto. It will be appreciated that various changes and modifications can be made in the invention within the scope not departing from the gist thereof.

For example, in the foregoing embodiment, the specific description has been given mainly to the N-channel power JFET, but the present invention is not limited thereto. It will be appreciated that the present invention is also applicable to a P-channel power JFET. Also, in the foregoing embodiment, the specific description has been given mainly to the normally-off power JFET, but the present invention is not limited thereto. It will be appreciated that the present invention is also applicable to a normally-on power JFET. Also, in the foregoing embodiment, the specific description has been given mainly to the power JFET, but the present invention is not limited thereto. It will be appreciated that the present invention is also applicable to a power MISFET (Metal Insulator Semiconductor Field Effect Transistor) or MOSFET (Metal Oxide Semiconductor Field Effect Transistor). Also, in the foregoing embodiment, the specific description has been given mainly to the active device (such as FET, IGBT, or diode) using the silicon-carbide-based semiconductor substrate (the polytype of which is not limited to 4H, and may also be another) such as SIC, but the present invention is not limited thereto. It will be appreciated that the present invention is also applicable to a GaN-based active device.

What is claimed is:

1. A method of manufacturing a junction field effect transistor, comprising the steps of:

(a) providing on a first main surface of a silicon-carbide-based semiconductor substrate having a first conductivity type, a first silicon-carbide-based semiconductor epitaxial layer having the first conductivity type and a lower impurity concentration than the semiconductor substrate;

(b) forming a first structure having a plurality of first gate impurity regions by doping a surface of the first silicon-carbide-based semiconductor epitaxial layer with an impurity having a second conductivity type by ion implantation to introduce, into the surface of the first epitaxial layer, the plurality of first gate impurity regions;

(c) after the step (b), performing first activation annealing on the first structure;

(d) after the step (c), forming, on the surface of the first epitaxial layer , a second silicon-carbide-based semiconductor epitaxial layer having the first conductivity type and a lower impurity concentration than the semiconductor substrate;

(e) forming a second structure having a plurality of second gate impurity regions by doping a surface of the second silicon-carbide-based semiconductor epitaxial layer with an impurity having the second conductivity type by ion implantation to introduce, into the surface of the second epitaxial layer, the plurality of second gate impurity regions respectively coupled to the plurality of first gate impurity regions;

(f) after the step (e), performing second activation annealing on the second structure;

(g) after the step (f), forming, over the second epitaxial layer, a third silicon-carbide-based semiconductor epitaxial layer having the first conductivity type and a lower impurity concentration than the semiconductor substrate;

(h) forming a third structure having a plurality of third gate impurity regions by doping a surface of the third silicon-carbide-based semiconductor epitaxial layer with an impurity having the second conductivity type by ion implantation to introduce, into the surface of the third epitaxial layer, the plurality of third gate impurity regions respectively coupled to the plurality of second gate impurity regions;

(i) after the step (h), performing third activation annealing on the third structure; and

(j) after the step (i), forming a source region of the first conductivity type between adjacent third gate impurity regions in the third epitaxial layer,

wherein a spacing between the third gate impurity regions is larger than a spacing between the second gate impurity regions.

2. A method of manufacturing a junction field effect transistor according to claim **1**,

wherein the first activation annealing and the second activation annealing are each performed in a state where the first main surface of the semiconductor substrate is covered with a carbon-based film.

3. A method of manufacturing a junction field effect transistor according to claim **2**,

wherein the third activation annealing is performed in a state where the first main surface of the semiconductor substrate is covered with a carbon-based film.

4. A method of manufacturing a junction field effect transistor according to claim **1**,

wherein the plurality of third gate impurity regions are respectively coupled directly to the plurality of second gate impurity regions.

5. A method of manufacturing a junction field effect transistor according to claim **1**,

wherein the plurality of third gate impurity regions are respectively coupled to the plurality of second gate impurity regions through intervening gate regions formed in a further silicon-carbide-based semiconductor epitaxial layer formed between the second and third epitaxial layers and having the first conductivity type and a lower impurity concentration than the semiconductor substrate.

6. A method of manufacturing a junction field effect transistor, comprising:

successively forming, over a first main surface of a silicon-carbide-based semiconductor substrate having a first conductivity type, a plurality of structures each including a respective silicon-carbide-based semiconductor epitaxial layer having the first conductivity type and a lower impurity concentration than the semicon-